Bab 2: Akusisi Sinyal dan Jenis Sinyal

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Signal

- Continues-time (analog) signals
- Discrete-time signals
- Digital Signal

Real-time DSP

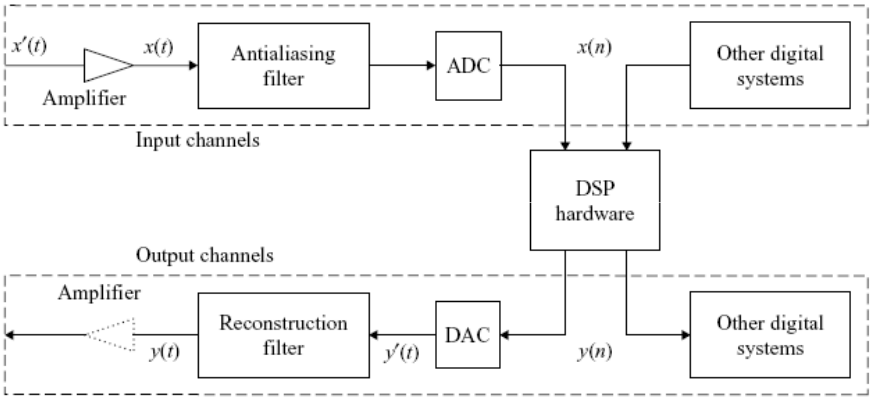


Figure 1.1 Basic functional block diagram of a real-time DSP system

Analog Interface

Sampling

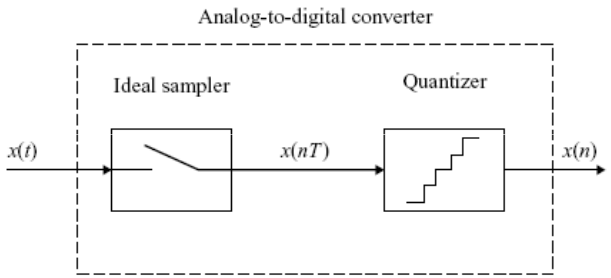


Figure 1.2 Block diagram of an ADC

$$T = \frac{1}{f_s},$$

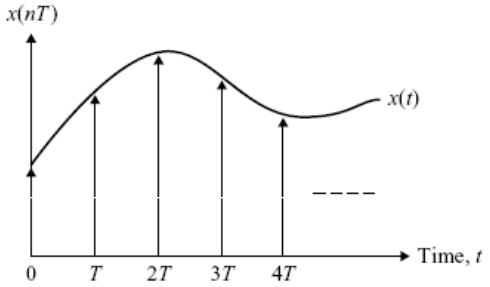
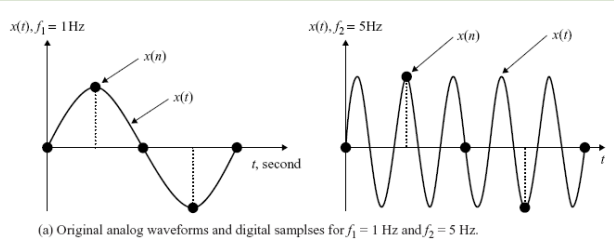


Figure 1.3 Example of analog signal $x(t)$ and discrete-time signal $x(nT)$

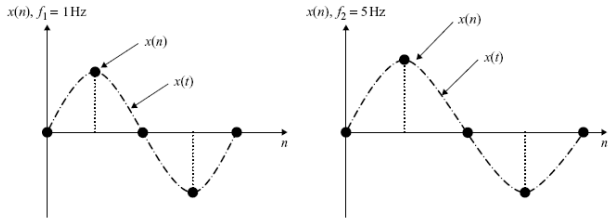
Shannon's Sampling Theorem

$$f_s \geq 2f_M,$$

Example



(a) Original analog waveforms and digital samplses for $f_1 = 1$ Hz and $f_2 = 5$ Hz.



(b) Digital samples for $f_1 = 1$ Hz and $f_2 = 5$ Hz and reconstructed waveforms.

Figure 1.4 Example of the aliasing phenomenon: (a) original analog waveforms and digital samples for $f_1 = 1$ and $f_2 = 5$ Hz; (b) digital samples of $f_1 = 1$ Hz and $f_2 = 5$ Hz and reconstructed waveforms

Filter Antialiasing

- Low Pass Filter,
  with cut off frequency

$$f_c \leq \frac{f_s}{2}.$$

Example Sampling Frequency

1. In International Telecommunication Union (ITU) speech compression standards, the sampling rate of ITU-T G.729 and G.723.1 is $f_s = 8$ kHz, thus the sampling period $T = 1/8000$ s $= 125\ \mu$s. Note that $1\ \mu s = 10^{-6}$ s.

2. Wideband telecommunication systems, such as ITU-T G.722, use a sampling rate of $f_s = 16$ kHz, thus $T = 1/16\,000$ s $= 62.5\ \mu$s.

3. In audio CDs, the sampling rate is $f_s = 44.1$ kHz, thus $T = 1/44\,100$ s $= 22.676\ \mu$s.

4. High-fidelity audio systems, such as MPEG-2 (moving picture experts group) AAC (advanced audio coding) standard, MP3 (MPEG layer 3) audio compression standard, and Dolby AC-3, have a sampling rate of $f_s = 48$ kHz, and thus $T = 1/48\,000$ s $= 20.833\ \mu$s. The sampling rate for MPEG-2 AAC can be as high as 96 kHz.

Quantization and Encoding

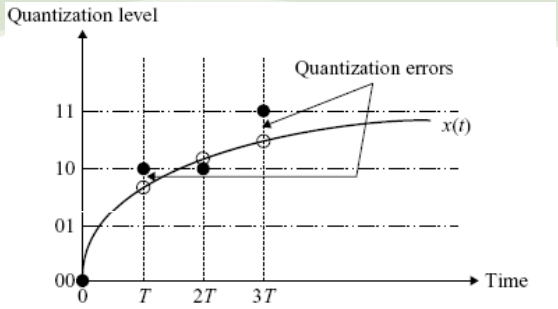


Figure 1.5 Digital samples using a 2-bit quantizer

1. An 8-bit ADC with 256 (2^8) levels can only provide 19.5 mV resolution and 48 dB SQNR.
2. A 12-bit ADC has 4096 (2^{12}) levels of 1.22 mV resolution, and provides 72 dB SQNR.
3. A 16-bit ADC has 65 536 (2^{16}) levels, and thus provides 76.294 μV resolution with 96 dB SQNR.

Smoothing Filter

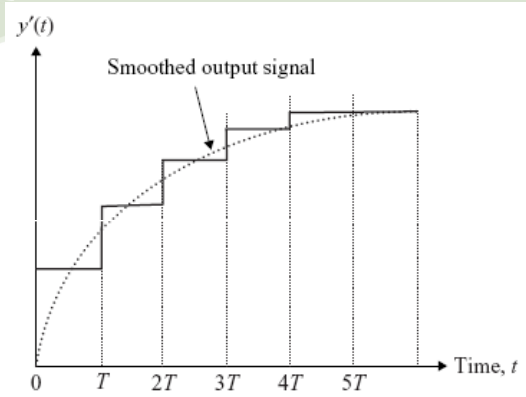


Figure 1.6 Staircase waveform generated by a DAC

Data Converters

- analog interface chip (AIC) or coder/decoder (CODEC):
  Integrated with antialiasing filter, an ADC, a DAC, and a reconstruction filter all on a single piece of silicon
- Example : Texas Instruments' TLV320AIC23 (AIC23) chip

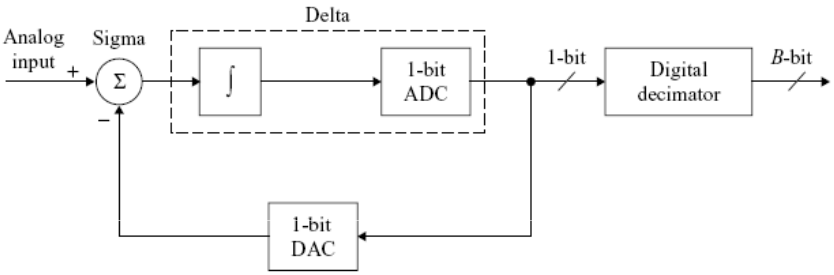


Figure 1.7 A conceptual sigma–delta ADC block diagram

DSP Processor

- Microprocessor optimized for processing repetitive numerically intensive operations at high rates. DSP processors with architectures and instruction sets specifically designed for DSP applications are manufactured by Texas Instruments, Freescale, Agere, Analog Devices, and many others

- Five hardware platforms are widely used for DSP systems:
  1. special-purpose (custom) chips such as application-specific integrated circuits (ASIC);
  2. field-programmable gate arrays (FPGA);
  3. general-purpose microprocessors or microcontrollers (*μP/μC);*
  4. general-purpose digital signal processors (DSP processors); and
  5. DSP processors with application-specific hardware (HW) accelerators

Table 1.2 Current commercially available DSP processors

Vendor	Family	Arithmetic type	Clock speed
Texas instruments	TMS320C24x	Fixed-point	40 MHz
	TMS320C28x	Fixed-point	150 MHz
	TMS320C54x	Fixed-point	160 MHz
	TMS320C55x	Fixed-point	300 MHz
	TMS320C62x	Fixed-point	300 MHz
	TMS320C64x	Fixed-point	1 GHz
	TMS320C67x	Floating-point	300 MHz
Analog devices	ADSP-218x	Fixed-point	80 MHz
	ADSP-219x	Fixed-point	160 MHz
	ADSP-2126x	Floating-point	200 MHz
	ADSP-2136x	Floating-point	333 MHz
	ADSP-BF5xx	Fixed-point	750 MHz
	ADSP-TS20x	Fixed/Floating	600 MHz
Freescale	DSP56300	Fixed, 24-bit	275 MHz
	DSP568xx	Fixed-point	40 MHz
	DSP5685x	Fixed-point	120 MHz
	MSC71xx	Fixed-point	200 MHz
	MSC81xx	Fixed-point	400 MHz
Agere	DSP1641x	Fixed-point	285 MHz

Source: Adapted from [11]

DSP Features

- **Fast MAC units**
- **Multiple memory accesses**
- **Special addressing modes**
- **Special program control**
- **Optimize instruction set**
- **Effective peripheral interface**

Fixed- and Floating-Point Processors

- Fixed-point DSP processors are either 16-bit or 24-bit devices, while floating-point processors are usually 32-bit devices. A typical 16-bit fixed-point processor, such as the TMS320C55x, stores numbers in a 16-bit integer or fraction format in a fixed range.

Example 1.7: The precision and dynamic range of commonly used 16-bit fixed-point processors are summarized in the following table:

	Precision	Dynamic range
Unsigned integer	1	$0 \le x \le 65\,535$
Signed integer	1	$-32\,768 \le x \le 32\,767$
Unsigned fraction	2^{-16}	$0 \le x \le (1 - 2^{-16})$
Signed fraction	2^{-15}	$-1 \le x \le (1 - 2^{-15})$

The precision of 32-bit floating-point DSP processors is 2^{-23} since there are 24 mantissa bits. The dynamic range is $1.18 \times 10^{-38} \le x \le 3.4 \times 10^{38}$.

Real-Time Constraints

$$t_p + t_o < T,$$

$$f_M \le \frac{f_s}{2} < \frac{1}{2(t_p + t_o)}.$$

DSP System Design

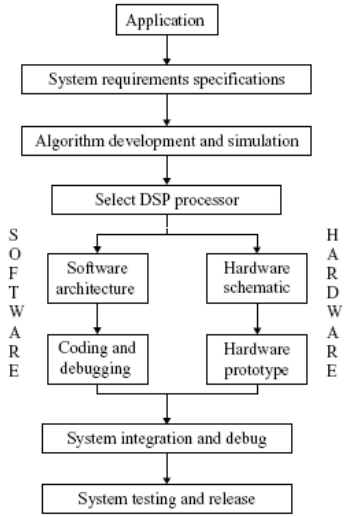


Figure 1.9 Simplified DSP system design flow

Algorithm Development

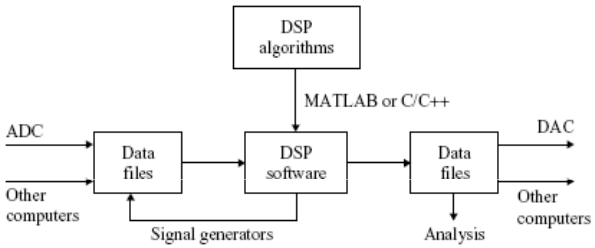


Figure 1.10 DSP software developments using a general-purpose computer

Selection of DSP Processors

- MIPS – millions of instructions per second;
- MOPS – millions of operations per second;
- MFLOPS – millions of floating-point operations per second;
- MHz – clock rate; and
- MMACS – millions of multiply–accumulate operations

Table 1.3 Some DSP applications with the relative importance rating

Application	Performance	Price	Power consumption
Audio receiver	1	2	3
DSP hearing aid	2	3	1
MP3 player	3	1	2
Portable video recorder	2	1	3
Desktop computer	1	2	3
Notebook computer	3	2	1
Cell phone handset	3	1	2
Cellular base station	1	2	3

Source: Adapted from [12]
Note: Rating – 1–3, with 1 being the most important

High-Level Software Development Tools

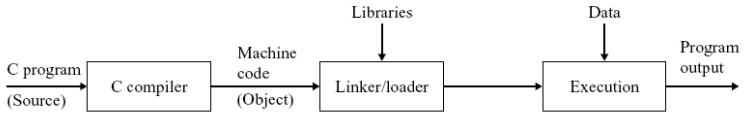


Figure 1.11 Program compilation, linking, and execution flow

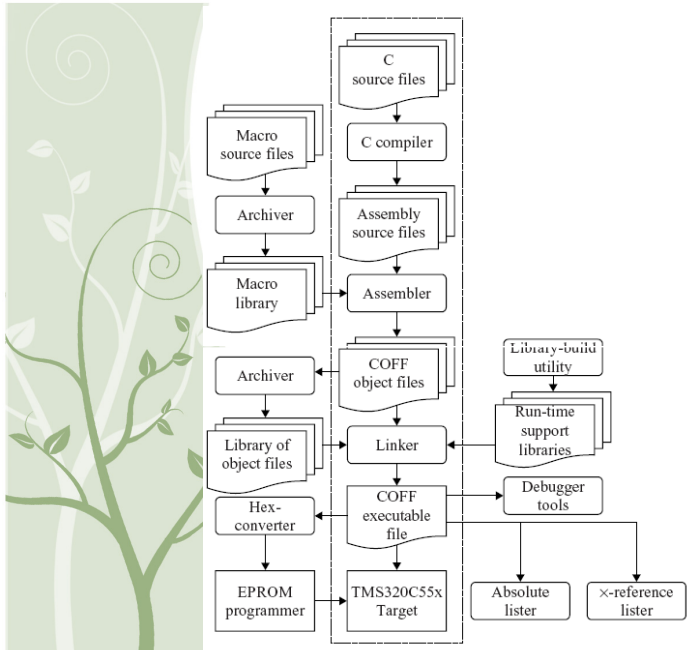


Figure 1.12 TMS320C55x software development flow and tools

Code Composer Studio (CCS) for Digital Signal Kit